Code No: 154AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, August/September - 2022
DIGITAL ELECTRONICS
(Electrical and Electronics Engineering)

Time: 3 Hours **Max.Marks:75**

Answer any five questions
All questions carry equal marks
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1.a) Define duality principal and explain it with the help of example. Find the complements of the functions $F_1 = x'yz' + x'y'z$ and $F_2 = x(y'z'+yz)$ by taking their duals and complementing each literal.
b) Implement the basic gates using Universal gates. [8+7]

2.a) Given a frame with bit sequence 1101011011 is transmitted and received as 1101011010. Determine the method of detecting the error using any one error detection method.
b) Explain in detail about TTL NAND gate with open collector output configuration. [8+7]

3.a) Simplify the following Boolean function F using K-Map
$F(A, B, C, D) = \sum m(1, 2, 3, 7, 8, 9, 10, 11, 14, 15)$
b) Simplify the function in SOP and POS using K-Map
$F(A,B,C,D,E)=\sum m(0,1,3,4,5,9,11,12,13,15)$ [7+8]

4.a) With a neat diagram, explain in detail about the working of a 4 bit look ahead adder. Also mention its advantages over conventional adder.
b) Design BCD to Excess-3 code converter and draw the logic diagram. [8+7]

5.a) Explain the working of the following:
i) S- R flip-flop ii) D flip-flop
b) With suitable logic diagram, explain a 4-bit bidirectional shift register. [6+9]

6.a) Design a 4-bit ring counter using D-Flip flop and explain its working.
b) Design and implement 3-bit ripple counter using J-K flip flop. [8+7]

7.a) Explain a weighted resistor DAC in detail? Also give its limitations.
b) Explain successive approximation ADC with an example. [8+7]

8.a) What is memory decoding? Explain about the construction of 4 × 4 RAM.
b) Explain in detail about the programmable logic devices. [8+7]

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